Enrollment No: _____ Exam Seat No:_____

C. U. SHAH UNIVERSITY

Summer Examination-2020

Subject Name: VLSI Technology

Subject Code: 4TE07VLT1 Branch: B.Tech (EC)

Semester: 7 Date: 27/02/2020 Time: 10:30 To 01:30 Marks: 70

Instructions:

(1) Use of Programmable calculator & any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

Q-1 Attempt the following questions **(14)**

a) Draw the more simplified view of VLSI design flow.
b) Discuss briefly term design hierarchy.
c) Discuss briefly term regularity.
d) Discuss briefly term modularity.
e) Discuss briefly term locality.
f) State the different VLSI design styles.
g) State the names of components in typical FPGA chip.
h) What is the difference between positive photoresist and negative photoresist?
i) Why do we require device isolation between MOS transistors that comprise an IC?
j) Discuss briefly short channel effect.
k) Discuss briefly narrow channel effect.
l) Draw the three stage ring oscillator circuit consisting of identical inverts.
m) Draw general layout of an H-tree clock distribution network.
n) Discuss controllability in brief.

Attempt any four questions from Q-2 to Q-8

Q-2 Attempt all questions **(14)**

a) Which are the four general criteria to measure design quality of a fabricated integrated circuit (chip)? Briefly explain each of them. **07**
b) Discuss VLSI Design flow in detail with diagrams. **07**

Q-3 Attempt all questions **(14)**

a) Describe the process of fabrication of the NMOS transistor. **07**
b) Discuss various packaging technology used for VLSI chips. **07**

Q-4 Attempt all questions **(14)**

a) Define threshold voltage (V_T) of MOSFET device. Which are the four physical components on which V_T depends? Derive expression for V_T. **07**
b) What is the need of scaling? Discuss constant field scaling in detail with its merits and demerits. **07**

Q-5 Attempt all questions **(14)**

a) Draw CMOS Inverter circuit. Obtain expressions for V_{IL} and V_{IH}. **07**

	b)	Describe Elmore Delay technique to estimate the delay of interconnects.	**07**
Q-6		**Attempt all questions**	**(14)**
	a)	Explain the CMOS Transmission Gates (TGs). Draw eight-transistor CMOS – TG implementation of the XOR function.	**07**
	b)	Draw CMOS negative edge-triggered master-slave D flip-flop and explain its working.	**07**
Q-7		**Attempt all questions**	**(14)**
	a)	What is the need for voltage bootstrapping? Explain dynamic voltage bootstrapping circuit with necessary mathematical analysis.	**07**
	b)	What do you understand by clock skew? Explain various clock distribution schemes with diagrams.	**07**
Q-8		**Attempt all questions**	**(14)**
	a)	Discuss Ad hoc testable design techniques.	**07**
	b)	Explain Built-in Self Test (BIST) techniques with necessary diagrams.	**07**